Product Features

- QSFP-DD MSA compliant
- 100G Lambda MSA compliant
- 400GE FR4 specification compliant
- Non-hermetic package design
- 4 CWDM lanes MUX/DEMUX design
- 8 x 53.125 Gbps PAM4 electrical interface (400GAUI-8)
- Maximum power consumption 12 W
- LC duplex connector
- 425 Gbps aggregate bit rate
- Up to 2 km transmission on single mode fiber with FEC
- Single 3.3 V power supply
- RoHS compliant

Application

- Data Centers Network
- 400G Ethernet

Standards

- IEEE 802.3cu
- QSFP-DD MSA
- CMIS4.0

Description

The 400G QSFP-DD FR4 is a transceiver module designed for 2 km optical communication applications, and it is compliant with 100G Lambda MSA standard. This module can convert 8-channel 53.125 Gbps electrical data to 4-channel 106.25 Gbps optical signals, and multiplex them into a single channel for 425 Gbps optical transmission. Similarly, it optically de-multiplexes a 425 Gbps input into 4-channel signals, and converts them to 8-channel output electrical data on the receiver side. It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference. The module offers very high functionality and feature integration, accessible via the I2C interface. A block diagram is shown in Figure 1.

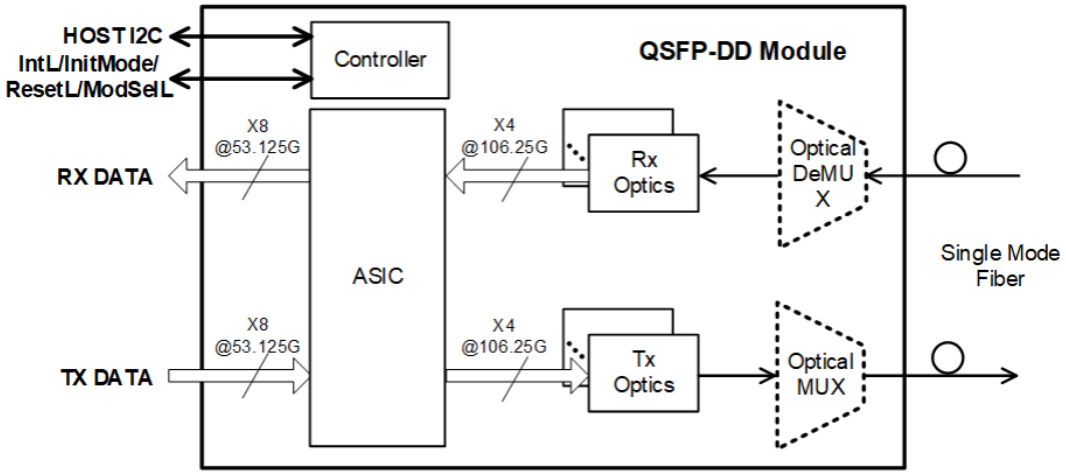


Figure 1 Transceiver block diagram

Absolute Maximum Ratings:

Module performance is not guaranteed and reliability is not implied for any condition that beyond the operating range. Exceeding the limits below may damage the transceiver module permanently.

Parameter	Unit	Min	Max
Case Operating Temperature	℃	0	+70
Storage Temperature Range	℃	-40	+85
Relative Humidity	%	0	85
Power Supply Voltage	V	-0.3	+3.6

Recommended Operating Conditions:

Parameter	Min	Typ	Max	Unit
Operating Case Temperature Range	0		70	˚C
Power Supply Voltage	3.135	3.3	3.465	V
Data Rate accuracy	-100		100	ppm
Link distance with G.652	0.5		2000	m

Electrical Characteristics:

Parameter	Unit	Min	Typ	Max	Notes
Supply Current	A			3.64	
Power Consumption	W			12	
Receiver					
Data rate, each lane	GBd	26.5625 ± 100 ppm			
Overload differential voltage pk-pk	mV	900			
Common mode voltage	mV	-350		2850	
Differential termination resistance mismatch	%			10	At 1 MHz
Differential return loss (SDD11)	dB	Equation(16-1)			OIF-CEI-56G-VSR PAM4
Common mode to differential mode conversion (SCD11)	dB	Equation(16-2)			OIF-CEI-56G-VSR PAM4
Transmitter					
Data rate, each lane	GBd	26.5625 ± 100 ppm			
Differential voltage, pk-pk	mV			900	
Common mode voltage (Vcm)	mV	-300		2850	
Common mode noise, RMS	mV			17.5	
Differential termination resistance mismatch	%			10	At 1 MHz
Differential return loss (SDD22)	dB			Equation(16-1)	
Common mode to differential mode conversion (SCD22)	dB			Equation(16–3)	
Common mode return loss(SCC22)	dB			-2	From 250 MHz to 19 GHz
Transition time	ps	9.5			
Near-end eye width at 10-6 probability (EW6)	UI	0.265			
Near-end eye height at 10-6 probability (EH6)	mV	70			
Far-end eye width at 10-6 probability (EW6)	UI	0.2			
Far-end eye height at 10-6 probability (EH6)	mV	30			
Near-end eye linearity		0.85			

Optical Characteristics:

Parameter	Unit	Min	Typ	Max	Notes
Transmitter					
Data rate, each Lane	GBd	53.125 ± 100 ppm			
Modulation format		PAM4			
Line wavelengths	nm	1264.5	1271	1277.5	
		1284.5	1291	1297.5	
		1304.5	1311	1317.5	
		1324.5	1331	1337.5	
Total average launch power	dBm			9.5	
Average launch power, each lane	dBm	-3.3		3.5	
Optical modulation amplitude (OMA), each lane	dBm	-0.2		3.7	
Extinction ratio (ER)	dB	3.5			
Side-mode suppression ratio (SMSR)	dB	30			
Launch power in OMA minus TDECQ, each lane	dBm	-1.6			
Transmitter and dispersion eye closure for PAM4, each Lane (TDECQ)	dB			3.4	
Difference in launch power between any two lanes (OMA outer)	dB			4	
RIN17.1OMA	dB/Hz			-136	
Optical return loss tolerance	dB			17.1	
Transmitter reflectance	dB			-26	
Receiver					
Data rate, each Lane	dB	53.125 ± 100 ppm			
Modulation format		PAM4			
Damage threshold, each lane	dBm	4			
Line wavelengths	nm	1264.5	1271	1277.5	
		1284.5	1291	1297.5	
		1304.5	1311	1317.5	
		1324.5	1331	1337.5	
Average receiver power, each lane	dBm	-7.3		3.5	

Receiver power, each lane (OMA)	dBm			3.7	
Difference in receiver power between any two lanes (OMA)	dB			4.1	
Receiver sensitivity (OMA outer), each lane (max)	dBm	See Note			
LOS assert	dBm	-20			
LOS de-assert	dBm			-8.6	
LOS hysteresis	dB	0.5			
Receiver reflectance	dB			-26	

Note:

Measured with conformance test signal for BER = 2.4 x 10 - 4. A compliant receiver shall have stressed receiver sensitivity (OMA outer), each lane values below the mask of Figure 2, for SECQ values between 0.9 and 3.4 dB.

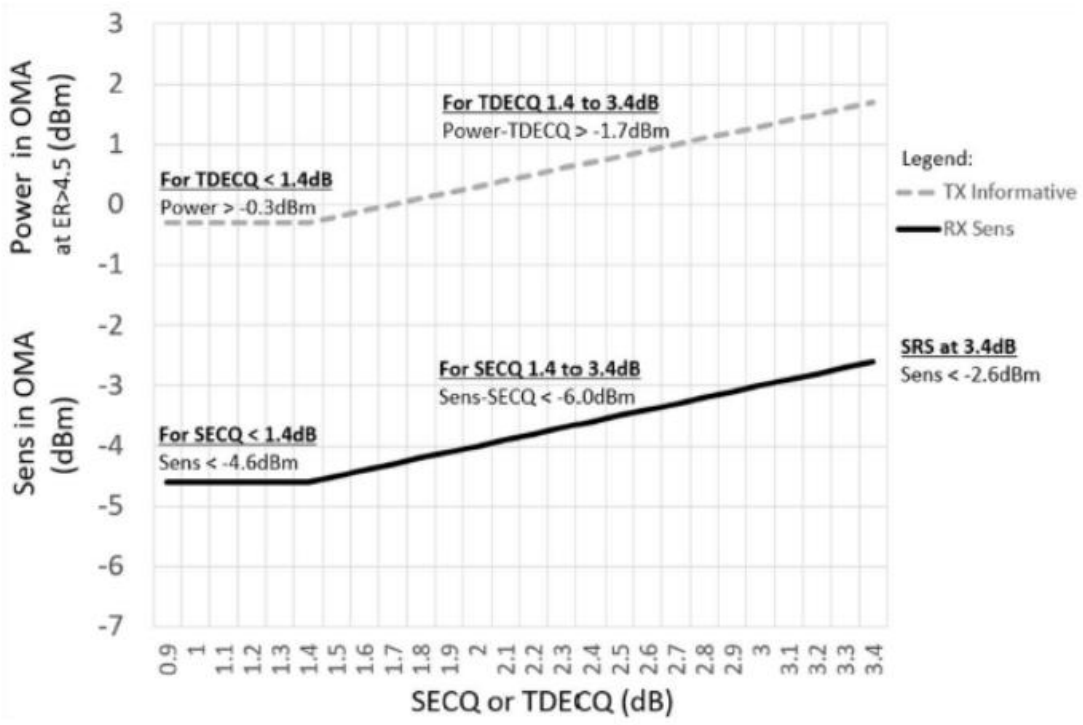


Figure 2 Stressed receiver sensitivity mask for 400GE-FR4

Pin Definition and Description

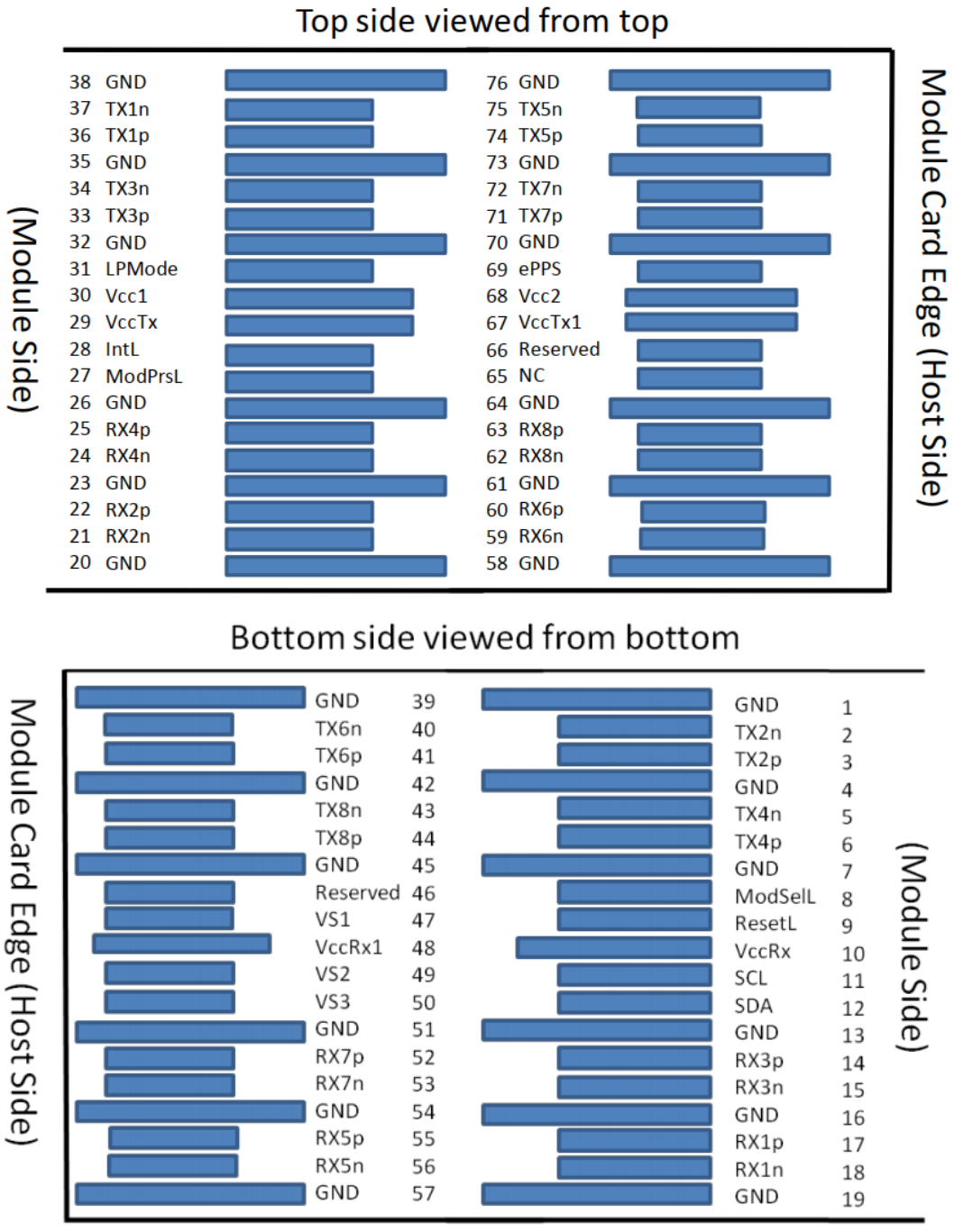


Table 1. Pin definition and descriptions

PIN	Symbol	Description	Plug Sequence[4]	Note
1	GND	Ground	1B	1
2	Tx2n	CML-I Transmitter 2 Inverted Data Input	3B	
3	Tx2p	CML-I Transmitter 2 Non-Inverted Data Input	3B	
4	GND	Ground	1B	1

5	Tx4n	CML-I Transmitter 4 Inverted Data Input	3B	
6	Tx4p	CML-I Transmitter 4 Non-Inverted Data Input	3B	
7	GND	Ground	1B	1
8	ModSelL	LVTLL-I Module Select	3B	
9	ResetL	LVTLL-I Module Reset	3B	
10	VCCRx	+3.3V Power Supply Receiver	2B	2
11	SCL	LVCMOS-I/O 2-Wire Serial Interface Clock	3B	
12	SDA	LVCMOS-I/O 2-Wire Serial Interface Data	3B	
13	GND	Ground	1B	1
14	Rx3p	CML-O Receiver 3 Non-Inverted Data Output	3B	
15	Rx3n	CML-O Receiver 3 Inverted Data Output	3B	
16	GND	Ground	1B	1
17	Rx1p	CML-O Receiver 1 Non-Inverted Data Output	3B	
18	Rx1n	CML-O Receiver 1 Inverted Data Output	3B	
19	GND	Ground	1B	1
20	GND	Ground	1B	1
21	Rx2n	CML-O Receiver 2 Inverted Data Output	3B	
22	Rx2p	CML-O Receiver 2 Non-Inverted Data Output	3B	
23	GND	Ground	1B	1
24	Rx4n	CML-O Receiver 4 Inverted Data Output	3B	
25	Rx4p	CML-O Receiver 4 Non-Inverted Data Output	3B	
26	GND	Ground	1B	1
27	ModPrsL	Module Present	3B	
28	IntL	Interrupt	3B	
29	VCCTx	+3.3V Power Supply Transmitter	2B	2
30	VCC1	+3.3V Power Supply	2B	2
31	LPMode	LVTLL-I Low Power Mode	3B	
32	GND	Ground	1B	1
33	Tx3p	CML-I Transmitter 3 Non-Inverted Data Input	3B	
34	Tx3n	CML-I Transmitter 3 Inverted Data Input	3B	
35	GND	Ground	1B	1
36	Tx1p	CML-I Transmitter 1 Non-Inverted Data Input	3B	
37	Tx1n	CML-I Transmitter 1 Inverted Data Input	3B	
38	GND	Ground	1B	1
39	GND	Ground	1A	1
40	Tx6n	CML-I Transmitter 6 Inverted Data Input	3A	
41	Tx6p	CML-I Transmitter 6 Non-Inverted Data Input	3A	
42	GND	Ground	1A	1
43	Tx8n	CML-I Transmitter 8 Inverted Data Input	3A	
44	Tx8p	CML-I Transmitter 8 Non-Inverted Data Input	3A	
45	GND	Ground	1A	1
46	Reserved	For future use	3A	3
47	VS1	Module vendor specific 1	3A	3
48	VCCRx1	+3.3V Power Supply Receiver	2A	2
49	VS2	Module vendor specific 2	3A	3
50	VS3	Module vendor specific 3	3A	3

51	GND	Ground	1A	1
52	Rx7p	CML-O Receiver 7 Non-Inverted Data Output	3A	
53	Rx7n	CML-O Receiver 7 Inverted Data Output	3A	
54	GND	Ground	1A	1
55	Rx5p	CML-O Receiver 5 Non-Inverted Data Output	3A	
56	Rx5n	CML-O Receiver 5 Inverted Data Output	3A	
57	GND	Ground	1A	1
58	GND	Ground	1A	1
59	Rx6n	CML-O Receiver 6 Inverted Data Output	3A	
60	Rx6p	CML-O Receiver 6 Non-Inverted Data Output	3A	
61	GND	Ground	1A	1
62	Rx8n	CML-O Receiver 8 Inverted Data Output	3A	
63	Rx8p	CML-O Receiver 8 Non-Inverted Data Output	3A	
64	GND	Ground	1A	1
65	NC	No connect	3A	3
66	Reserved	For future use	3A	3
67	VCCTx1	+3.3V Power Supply Transmitter	2A	2
68	VCC2	+3.3V Power Supply	2A	2
69	ePPS	Precision Time Protocol (PTP) reference clock input	3A	3
70	GND	Ground	1A	1
71	Tx7p	CML-I Transmitter 7 Non-Inverted Data Input	3A	
72	Tx7n	CML-I Transmitter 7 Inverted Data Input	3A	
73	GND	Ground	1A	1
74	Tx5p	CML-I Transmitter 5 Non-Inverted Data Input	3A	
75	Tx5n	CML-I Transmitter 5 Inverted Data Input	3A	
76	GND	Ground	1A	1

Note 1: QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to the potential unless otherwise noted. Connect these directly to the host board signal common ground plane.

Note 2: VccRx,VccRx1,Vcc1,Vcc2,VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 7. VccRx, VccRx1,Vcc1,Vcc2,VccTx and VccTx1 may be internally connected with the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000mA.

Note 3: All Vendor Specific, Reserved ,No Connect and ePPS (if not used) pins may be terminated with 50 Ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

Note 4: plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A,2A,3A,1B,2B,3B. (see figure for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A,1B will then occur simultaneously, followed by 2A,2B,followed by 3A,3B.

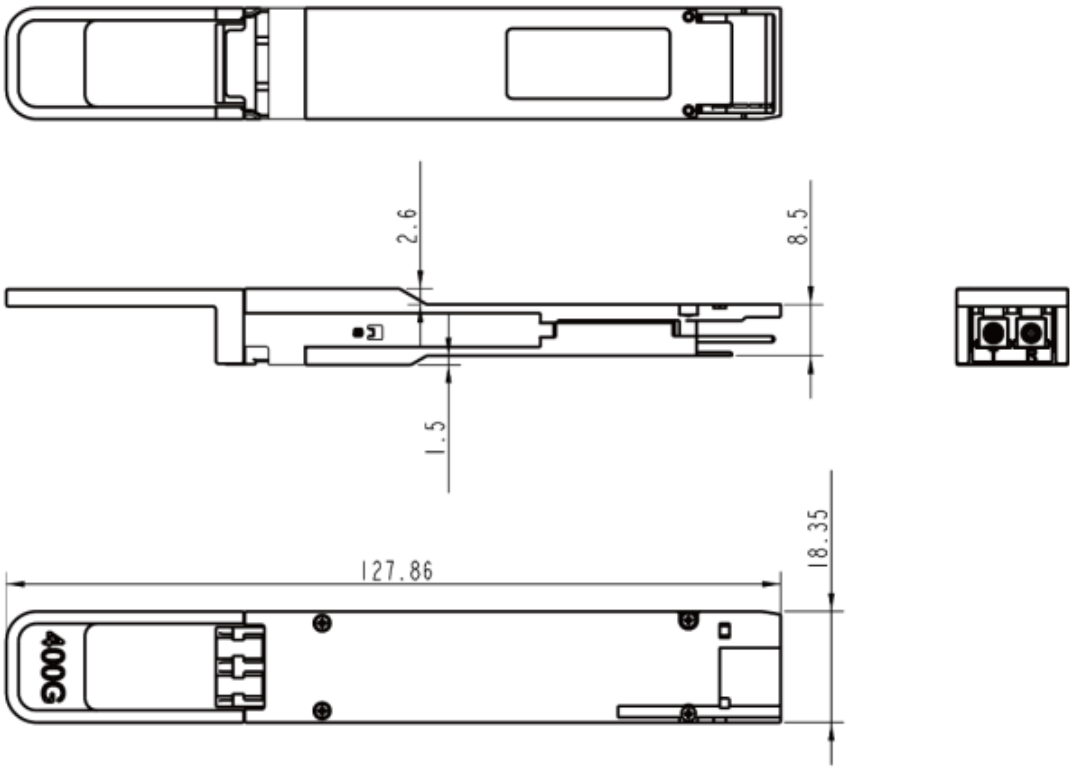
Digital Diagnostic Monitoring Functions

400G QSFP-DD FR4 supports the I2C-based Diagnostic Monitoring Interface (DMI) defined in document QSFP-DD-CMIS-rev4p0. The host can access real-time performance of transmitter and receiver optical power, temperature, supply voltage and bias current.

Parameter	Data address		
	Alarm & Warning	**Alarm & Warning thresholds**	**Monitor**
Module temperature	Lower page 9	Page2h (128-135)	Lower page (14-15)
Module Voltage	Lower page 9	Page2h (136-143)	Lower page (16-17)
Bias current	Page11h(143-146)	Page2h (184-191)	Page11h (170-177)
Transmitter optical power	Page11h(139-142)	Page2h (176-183)	Page11h (154-161)
Receiver optical power	Page11h(149-152)	Page2h (192-199)	Page11h (186-193)

Mechanical Specifications

Compatible with the QSFP-DD Type 2 Specification for pluggable form factor modules.



ESD Information

Normal ESD precautions are required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and otherwise handled in an ESD protected environment utilizing standard grounded benches, floor mats, and wrist straps.

Parameter	Threshold	Note
ESD of high-speed pins	1kV	Human body model
ESD of low-speed pins	2kV	Human body model
Air discharge during operation	15kV	
Direct contact discharges to the case	8kV	