

Product Features

- Compliant to OSFP MSA 5.0
- Compliant with CMIS 4.0
- 8x106. 25Gb/s Electrical Interface (800GAUI-8)
- Maximum Power Consumption 16W
- Case Temperature Range: 0 to 70°C
- RoHS Complaint
- Up to 106.25 Gbps Data Rate Per Channel by PAM4 Modulation
- Maximum link length of 30m on OM3 Multimode Fiber (MMF) and 50m on OM4 MMF with FEC
- Support 800GAUI-8 Electrical Interface
- Integrated 850nm VCSEL Array and PD Array
- DDM Function Implemented
- Hot-pluggable
- Single +3.3V Power Supply

Application

- Networks
- Data Centers and Cloud

Description

The 800GBASE-SR8 OSFP Optical Transceiver Module is designed for use in 800Gb/s systems throughput up to 30m over OM3 or 50m over OM4 multimode fiber (MMF) using a wavelength of 850nm via dual MTP/MPO-12 connectors. Digital diagnostics functions are also available via the I2C interface, as specified by the OSFP MSA, to allow access to real time operating parameters. With these features, this easy to install, hot swappable transceiver is suitable to be used in various applications, such as data centers, high-performance computing networks, enterprise core and distribution layer applications.

Absolute Maximum Ratings

Parameter	Unit	Min	Max
Storage Temperature Range	°C	-40	85
Supply Voltage	V	0	4



Parameter	Unit	Min	Max
Relative Humidity (Non-condensing)	%	5	85

Recommended Operating Conditions:

Parameter	Unit	Min	Max
Case Temperature-Operating	°C	0	70
Supply Voltage	V	3.135	3.465
Power Consumption	W		16
Pre-FEC Bit Error Ratio			2.4*10-4

Optical Characteristics

Parameter	ameter Unit Min. Typical				
Transmitter					
Signaling Rate, Each Lane	GBd	53.125 ± 100 ppm			
Lane Wavelength Range	nm		850		
RMS Spectral Width	nm			0.6	
Modulation Format			PAM4		
Average Optical Power Per Lane	dBm	-4.6		4	
Outer Optical Modulation Amplitude (ON	lAouter), Eac	h Lane			
for TDECQ≤1.8dB	dBm	-2.6		3.5	
for 1.8 <tdecq≤4.4db< td=""><td>dBm</td><td>-4.4+TDECQ</td><td></td><td>3.5</td></tdecq≤4.4db<>	dBm	-4.4+TDECQ		3.5	
Outer Optical Modulation Amplitude (ON	lAouter), Eac	h Lane			
for TDECQ≤1.8dB	dBm	-2.6		3.5	
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Transmitter and Dispersion Eye Closure for	dB			4.4	
PAM4, Each Lane				7.7	
Transmitter Eye Closure for PAM4 (TECQ),	dB			4.4	
Each Lane					
ER	dB	2.5			
Transmitter Excursion, Each Lane	dB			2	
Transmitter Transition Time, Each Lane	ps			17	
Average Launch Power Per Lane @ TX Off	dBm			-30	
State					
Relative Intensity Noise12 (OMA)	dB/Hz			-131	
Optical Return Loss Tolerance	dB			12	
Encircled Flux	dB			>=86%at 19µm	
LITORIOIGA FIGA	QD			<=30% at	



				4.5µm		
Receiver						
Signaling Rate Each Lane	GBd		53.125±100ppm			
Lane Wavelength Range	nm			850		
Modulation Format			PAM4			
Damage Threshold	dBm	5				
Average Receive Power, Each Lane	dBm	-6.4		4		
Receiver Power, Each Lane (OMA)	dBm			3.5		
Receiver Sensitivity Each Lane (OMAout	Receiver Sensitivity Each Lane (OMAouter)					
for TDECQ≤1.8dB	dBm			-4.6		
for 1.8 <tdecq≤4.4db< td=""><td>dBm</td><td></td><td></td><td>-6.4+TDECQ</td></tdecq≤4.4db<>	dBm			-6.4+TDECQ		
Receiver Reflectance	dB			-12		
Stressed Receiver Sensitivity (OMAouter),	dBm			-2		
Each Lane						
Stressed Conditions for Stress Receiver Sensitivity						
Stressed Eye Closure for PAM4 (SECQ), Lane under Test	dB		4.4			
OMAouter of Each Aggressor Lane	dBm		3.5			

Electrical Specifications

Parameter	Unit	Min.	Тур.	Max.	
Transmitter Electrical Input Characteris	tics at TP	1			
Signaling Rate, Per Lane	GBd		53.125		
Differential Pk-pk Input Voltage Tolerance	mV	900			
Common-mode to Differential Return Loss		802.3ck Equation(120G-1)			
Differential Termination Mismatch	%			10	
Module Stressed Input Test		See 120G.3.4.1			
Single-ended Voltage Tolerance Range	V	-0.4	-0.4		
DC Common-mode Voltage	mV	-350		2850	
Receiver Electrical Output Characterist	ics at TP4				
Signaling Rate Per Lane	GBd		53.125		
AC common-mode Output Voltage(RMS)	mV			17.5	
Differential Peak-to-peak Output Voltage	dB			900	
Near-end ESMW (Eye Symmetry Mask Width)	UI		TBD		
Near-end Eyeheight, Differential	mV	24			



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Near-end Vertical Eye Closure	dB			7.5
Far-end Eyeheight, Differential	mV	24		
Far-end Vertical Eye Closure	dB			7.5
Differential Termination Mismatch	%			10
Single-ended Voltage Tolerance Range	V	-0.4		3.3
DC Common-mode Voltage	mV	-350		2850
Receiver Electrical Output Characteristics at TP4				
Signaling Rate Per Lane	GBd		53.125	
AC common-mode Output Voltage(RMS)	mV			17.5
Differential Peak-to-peak Output Voltage	dB			900
Near-end Eyeheight, Differential	mV	24		
Near-end Vertical Eye Closure	dB			7.5
Differential Termination Mismatch	%			10
DC Common Mode Voltage	mV	-350		2850

Pin Definition and Description



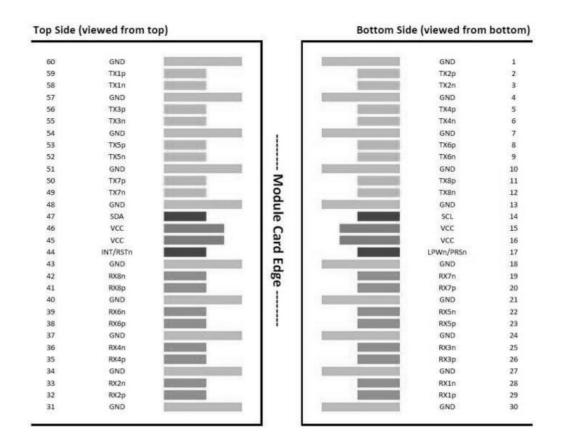


Table 1. Pin definition and descriptions

Pin	Symbol	Logic	Description	Note
1	GND		Ground	
2	TX2p	CML-I	Transmitted Data Non-Inverted	
3	TX2n	CML-I	Transmitted Data Inverted	
4	GND		Ground	
5	TX4p	CML-I	Transmitted Data Non-Inverted	
6	TX4n	CML-I	Transmitted Data Inverted	
7	GND		Ground	
8	TX6p	CML-I	Transmitted Data Non-Inverted	
9	TX6n	CML-I	Transmitted Data Inverted	
10	GND		Ground	
11	TX8p	CML-I	Transmitted Data Non-Inverted	
12	TX8n	CML-I	Transmitted Data Inverted	
13	GND		Ground	
14	SCL	LVCMOS-I/O	2-wire Serial Interface Clock	1
15	VCC		+3.3V Power	
16	VCC		+3.3V Power	



18	17	LPWn/PRSn	Multi-Level	Low-Power Mode / Module Present	2
20 RX7p CML-O Receiver Data Non-Inverted 21 GND Ground 22 RX5n CML-O Receiver Data Inverted 23 RX5p CML-O Receiver Data Non-Inverted 24 GND Ground 25 RX3n CML-O Receiver Data Inverted 26 RX3p CML-O Receiver Data Non-Inverted 27 GND Ground 28 RX 1n CML-O Receiver Data Non-Inverted 30 GND Ground 31 GND Ground 32 RX2p CML-O Receiver Data Non-Inverted 33 RX2n CML-O Receiver Data Inverted 34 GND Ground 35 RX4p CML-O Receiver Data Non-Inverted 36 RX4n CML-O Receiver Data Inverted 37 GND Ground 38 RX6p CML-O Receiver Data Inverted 40 GND Groun	18	GND		Ground	
21 GND Ground 22 RX5n CML-O Receiver Data Inverted 23 RX5p CML-O Receiver Data Inverted 24 GND Ground 25 RX3n CML-O Receiver Data Inverted 26 RX3p CML-O Receiver Data Non-Inverted 27 GND Ground 28 RX 1n CML-O Receiver Data Inverted 29 RX 1p CML-O Receiver Data Non-Inverted 30 GND Ground 31 GND Ground 32 RX2p CML-O Receiver Data Non-Inverted 33 RX2n CML-O Receiver Data Inverted 34 GND Ground 35 RX4p CML-O Receiver Data Inverted 36 RX4h CML-O Receiver Data Inverted 37 GND Ground 38 RX6p CML-O Receiver Data Non-Inverted 40 GND Ground	19	RX7n	CML-O	Receiver Data Inverted	
22 RX5p CML-O Receiver Data Inverted 23 RX5p CML-O Receiver Data Non-Inverted 24 GND Ground 25 RX3n CML-O Receiver Data Inverted 26 RX3p CML-O Receiver Data Non-Inverted 27 GND Ground 28 RX 1n CML-O Receiver Data Inverted 29 RX 1p CML-O Receiver Data Non-Inverted 30 GND Ground 31 GND Ground 32 RX2p CML-O Receiver Data Non-Inverted 33 RX2n CML-O Receiver Data Inverted 34 GND Ground 35 RX4p CML-O Receiver Data Inverted 36 RX4n CML-O Receiver Data Inverted 37 GND Ground 40 GND Ground 41 RX8p CML-O Receiver Data Inverted 42 RX8n CML-O	20	RX7p	CML-O	Receiver Data Non-Inverted	
23 RX5p CML-O Receiver Data Non-Inverted 24 GND Ground 25 RX3n CML-O Receiver Data Inverted 26 RX3p CML-O Receiver Data Non-Inverted 27 GND Ground 28 RX 1n CML-O Receiver Data Inverted 29 RX 1p CML-O Receiver Data Non-Inverted 30 GND Ground 31 GND Ground 32 RX2p CML-O Receiver Data Non-Inverted 33 RX2n CML-O Receiver Data Inverted 34 GND Ground 35 RX4p CML-O Receiver Data Non-Inverted 36 RX4n CML-O Receiver Data Inverted 37 GND Ground 38 RX6p CML-O Receiver Data Inverted 40 GND Ground 41 RX8p CML-O Receiver Data Inverted 42 RX8n CML-O </td <td>21</td> <td>GND</td> <td></td> <td>Ground</td> <td></td>	21	GND		Ground	
24 GND Ground 25 RX3n CML-O Receiver Data Inverted 26 RX3p CML-O Receiver Data Non-Inverted 27 GND Ground 28 RX1n CML-O Receiver Data Inverted 29 RX 1p CML-O Receiver Data Non-Inverted 30 GND Ground 31 GND Ground 32 RX2p CML-O Receiver Data Non-Inverted 33 RX2n CML-O Receiver Data Inverted 34 GND Ground 35 RX4p CML-O Receiver Data Inverted 36 RX4n CML-O Receiver Data Inverted 37 GND Ground 38 RX6p CML-O Receiver Data Inverted 40 GND Ground 41 RX8p CML-O Receiver Data Inverted 42 RX8n CML-O Receiver Data Inverted 43 GND Ground <	22	RX5n	CML-O	Receiver Data Inverted	
25 RX3n CML-O Receiver Data Inverted 26 RX3p CML-O Receiver Data Non-Inverted 27 GND Ground 28 RX 1n CML-O Receiver Data Inverted 29 RX 1p CML-O Receiver Data Non-Inverted 30 GND Ground 31 GND Ground 32 RX2p CML-O Receiver Data Non-Inverted 33 RX2n CML-O Receiver Data Inverted 34 GND Ground 35 RX4p CML-O Receiver Data Non-Inverted 36 RX4n CML-O Receiver Data Inverted 37 GND Ground 38 RX6p CML-O Receiver Data Inverted 40 GND Ground 41 RX8p CML-O Receiver Data Inverted 42 RX8n CML-O Receiver Data Inverted 43 GND Ground 44 INT/RSTn Multi-L	23	RX5p	CML-O	Receiver Data Non-Inverted	
26 RX3p CML-O Receiver Data Non-Inverted 27 GND Ground 28 RX 1n CML-O Receiver Data Inverted 29 RX 1p CML-O Receiver Data Non-Inverted 30 GND Ground 31 GND Ground 32 RX2p CML-O Receiver Data Non-Inverted 33 RX2n CML-O Receiver Data Inverted 34 GND Ground 35 RX4p CML-O Receiver Data Non-Inverted 36 RX4n CML-O Receiver Data Inverted 37 GND Ground 38 RX6p CML-O Receiver Data Inverted 40 GND Ground 41 RX8p CML-O Receiver Data Inverted 42 RX8n CML-O Receiver Data Inverted 43 GND Ground 44 INT/RSTn Multi-Level Module Interrupt / Module Reset 2 45	24	GND		Ground	
27 GND Ground 28 RX 1n CML-O Receiver Data Inverted 29 RX 1p CML-O Receiver Data Non-Inverted 30 GND Ground 31 GND Ground 32 RX2p CML-O Receiver Data Non-Inverted 33 RX2n CML-O Receiver Data Inverted 34 GND Ground 35 RX4p CML-O Receiver Data Non-Inverted 36 RX4n CML-O Receiver Data Inverted 37 GND Ground 38 RX6p CML-O Receiver Data Non-Inverted 40 GND Ground 41 RX8p CML-O Receiver Data Inverted 42 RX8n CML-O Receiver Data Inverted 42 RX8n CML-O Receiver Data Inverted 43 GND Ground 44 INT/RSTn Multi-Level Module Interrupt / Module Reset 2 45	25	RX3n	CML-O	Receiver Data Inverted	
28 RX 1p CML-O Receiver Data Inverted 29 RX 1p CML-O Receiver Data Non-Inverted 30 GND Ground 31 GND Ground 32 RX2p CML-O Receiver Data Non-Inverted 33 RX2n CML-O Receiver Data Inverted 34 GND Ground 35 RX4p CML-O Receiver Data Non-Inverted 36 RX4n CML-O Receiver Data Inverted 37 GND Ground 38 RX6p CML-O Receiver Data Non-Inverted 40 GND Ground 41 RX8p CML-O Receiver Data Inverted 42 RX8n CML-O Receiver Data Inverted 42 RX8n CML-O Receiver Data Inverted 43 GND Ground 44 INT/RSTn Multi-Level Module Interrupt / Module Reset 2 45 VCC +3.3V Power 46	26	RX3p	CML-O	Receiver Data Non-Inverted	
29 RX 1p CML-O Receiver Data Non-Inverted 30 GND Ground 31 GND Ground 32 RX2p CML-O Receiver Data Non-Inverted 33 RX2n CML-O Receiver Data Inverted 34 GND Ground 35 RX4p CML-O Receiver Data Non-Inverted 36 RX4n CML-O Receiver Data Inverted 37 GND Ground 38 RX6p CML-O Receiver Data Inverted 40 GND Ground 41 RX8p CML-O Receiver Data Inverted 42 RX8n CML-O Receiver Data Inverted 43 GND Ground 44 INT/RSTn Multi-Level Module Interrupt / Module Reset 2 45 VCC +3.3V Power 46 VCC +3.3V Power 47 SDA LVCMOS-I/O 2-wire Serial Interface Clock 1 48	27	GND		Ground	
30 GND	28	RX 1n	CML-O	Receiver Data Inverted	
31 GND Ground 32 RX2p CML-O Receiver Data Non-Inverted 33 RX2n CML-O Receiver Data Inverted 34 GND Ground 35 RX4p CML-O Receiver Data Non-Inverted 36 RX4n CML-O Receiver Data Inverted 37 GND Ground 38 RX6p CML-O Receiver Data Non-Inverted 39 RX6n CML-O Receiver Data Inverted 40 GND Ground 41 RX8p CML-O Receiver Data Inverted 42 RX8n CML-O Receiver Data Inverted 43 GND Ground 44 INT/RSTn Multi-Level Module Interrupt / Module Reset 2 45 VCC +3.3V Power 46 VCC +3.3V Power 47 SDA LVCMOS-I/O 2-wire Serial Interface Clock 1 48 GND Ground Transmitted Data Inverted	29	RX 1p	CML-O	Receiver Data Non-Inverted	
32 RX2p CML-O Receiver Data Non-Inverted 33 RX2n CML-O Receiver Data Inverted 34 GND Ground 35 RX4p CML-O Receiver Data Non-Inverted 36 RX4n CML-O Receiver Data Inverted 37 GND Ground 38 RX6p CML-O Receiver Data Non-Inverted 39 RX6n CML-O Receiver Data Inverted 40 GND Ground 41 RX8p CML-O Receiver Data Non-Inverted 42 RX8n CML-O Receiver Data Inverted 43 GND Ground 44 INT/RSTn Multi-Level Module Interrupt / Module Reset 2 45 VCC +3.3V Power 46 VCC +3.3V Power 47 SDA LVCMOS-I/O 2-wire Serial Interface Clock 1 48 GND Ground Transmitted Data Inverted 50 TX7p CML-I	30	GND		Ground	
33 RX2n CML-O Receiver Data Inverted 34 GND Ground 35 RX4p CML-O Receiver Data Non-Inverted 36 RX4n CML-O Receiver Data Inverted 37 GND Ground 38 RX6p CML-O Receiver Data Non-Inverted 39 RX6n CML-O Receiver Data Inverted 40 GND Ground 41 RX8p CML-O Receiver Data Inverted 42 RX8n CML-O Receiver Data Inverted 43 GND Ground 44 INT/RSTn Multi-Level Module Interrupt / Module Reset 2 45 VCC +3.3V Power 46 VCC +3.3V Power 47 SDA LVCMOS-I/O 2-wire Serial Interface Clock 1 48 GND Ground 49 TX7n CML-I Transmitted Data Inverted 50 TX7p CML-I Transmitted Data Inverted	31	GND		Ground	
34 GND Ground 35 RX4p CML-O Receiver Data Non-Inverted 36 RX4n CML-O Receiver Data Inverted 37 GND Ground 38 RX6p CML-O Receiver Data Non-Inverted 39 RX6n CML-O Receiver Data Inverted 40 GND Ground 41 RX8p CML-O Receiver Data Non-Inverted 42 RX8n CML-O Receiver Data Inverted 43 GND Ground 44 INT/RSTn Multi-Level Module Interrupt / Module Reset 2 45 VCC +3.3V Power 2 46 VCC +3.3V Power 4 47 SDA LVCMOS-I/O 2-wire Serial Interface Clock 1 48 GND Ground 3 49 TX7n CML-I Transmitted Data Inverted 50 TX7p CML-I Transmitted Data Inverted 51 GND G	32	RX2p	CML-O	Receiver Data Non-Inverted	
35 RX4p CML-O Receiver Data Non-Inverted 36 RX4n CML-O Receiver Data Inverted 37 GND Ground 38 RX6p CML-O Receiver Data Non-Inverted 39 RX6n CML-O Receiver Data Inverted 40 GND Ground 41 RX8p CML-O Receiver Data Inverted 42 RX8n CML-O Receiver Data Inverted 43 GND Ground 44 INT/RSTn Multi-Level Module Interrupt / Module Reset 2 45 VCC +3.3V Power 46 VCC +3.3V Power 47 SDA LVCMOS-I/O 2-wire Serial Interface Clock 1 48 GND Ground 49 TX7n CML-I Transmitted Data Inverted 50 TX7p CML-I Transmitted Data Inverted 51 GND Ground 52 TX5n CML-I Transmitted Data Inverted <td>33</td> <td>RX2n</td> <td>CML-O</td> <td>Receiver Data Inverted</td> <td></td>	33	RX2n	CML-O	Receiver Data Inverted	
36 RX4n CML-O Receiver Data Inverted 37 GND Ground 38 RX6p CML-O Receiver Data Non-Inverted 39 RX6n CML-O Receiver Data Inverted 40 GND Ground 41 RX8p CML-O Receiver Data Non-Inverted 42 RX8n CML-O Receiver Data Inverted 43 GND Ground 44 INT/RSTn Multi-Level Module Interrupt / Module Reset 2 45 VCC +3.3V Power 46 VCC +3.3V Power 47 SDA LVCMOS-I/O 2-wire Serial Interface Clock 1 48 GND Ground Ground 49 TX7n CML-I Transmitted Data Inverted 50 TX7p CML-I Transmitted Data Inverted 51 GND Ground 52 TX5n CML-I Transmitted Data Inverted	34	GND		Ground	
37 GND Ground 38 RX6p CML-O Receiver Data Non-Inverted 39 RX6n CML-O Receiver Data Inverted 40 GND Ground 41 RX8p CML-O Receiver Data Non-Inverted 42 RX8n CML-O Receiver Data Inverted 43 GND Ground 44 INT/RSTn Multi-Level Module Interrupt / Module Reset 2 45 VCC +3.3V Power 46 VCC +3.3V Power 47 SDA LVCMOS-I/O 2-wire Serial Interface Clock 1 48 GND Ground 49 TX7n CML-I Transmitted Data Inverted 50 TX7p CML-I Transmitted Data Non-Inverted 51 GND Ground 52 TX5n CML-I Transmitted Data Inverted	35	RX4p	CML-O	Receiver Data Non-Inverted	
38 RX6p CML-O Receiver Data Non-Inverted 39 RX6n CML-O Receiver Data Inverted 40 GND Ground 41 RX8p CML-O Receiver Data Non-Inverted 42 RX8n CML-O Receiver Data Inverted 43 GND Ground 44 INT/RSTn Multi-Level Module Interrupt / Module Reset 2 45 VCC +3.3V Power 46 VCC +3.3V Power 47 SDA LVCMOS-I/O 2-wire Serial Interface Clock 1 48 GND Ground 49 TX7n CML-I Transmitted Data Inverted 50 TX7p CML-I Transmitted Data Non-Inverted 51 GND Ground 52 TX5n CML-I Transmitted Data Inverted	36	RX4n	CML-O	Receiver Data Inverted	
39 RX6n CML-O Receiver Data Inverted 40 GND Ground 41 RX8p CML-O Receiver Data Non-Inverted 42 RX8n CML-O Receiver Data Inverted 43 GND Ground 44 INT/RSTn Multi-Level Module Interrupt / Module Reset 2 45 VCC +3.3V Power 46 VCC +3.3V Power 47 SDA LVCMOS-I/O 2-wire Serial Interface Clock 1 48 GND Ground Ground 49 TX7n CML-I Transmitted Data Inverted 50 TX7p CML-I Transmitted Data Non-Inverted 51 GND Ground 52 TX5n CML-I Transmitted Data Inverted	37	GND		Ground	
40 GND Ground 41 RX8p CML-O Receiver Data Non-Inverted 42 RX8n CML-O Receiver Data Inverted 43 GND Ground 44 INT/RSTn Multi-Level Module Interrupt / Module Reset 2 45 VCC +3.3V Power 2 46 VCC +3.3V Power 1 47 SDA LVCMOS-I/O 2-wire Serial Interface Clock 1 48 GND Ground 3 49 TX7n CML-I Transmitted Data Inverted 50 TX7p CML-I Transmitted Data Non-Inverted 51 GND Ground 52 TX5n CML-I Transmitted Data Inverted	38	RX6p	CML-O	Receiver Data Non-Inverted	
41 RX8p CML-O Receiver Data Non-Inverted 42 RX8n CML-O Receiver Data Inverted 43 GND Ground 44 INT/RSTn Multi-Level Module Interrupt / Module Reset 2 45 VCC +3.3V Power 4 46 VCC +3.3V Power 4 47 SDA LVCMOS-I/O 2-wire Serial Interface Clock 1 48 GND Ground 4 49 TX7n CML-I Transmitted Data Inverted 50 TX7p CML-I Transmitted Data Non-Inverted 51 GND Ground 52 TX5n CML-I Transmitted Data Inverted	39	RX6n	CML-O	Receiver Data Inverted	
42 RX8n CML-O Receiver Data Inverted 43 GND Ground 44 INT/RSTn Multi-Level Module Interrupt / Module Reset 2 45 VCC +3.3V Power 4 46 VCC +3.3V Power 4 47 SDA LVCMOS-I/O 2-wire Serial Interface Clock 1 48 GND Ground 4 49 TX7n CML-I Transmitted Data Inverted 50 TX7p CML-I Transmitted Data Non-Inverted 51 GND Ground 52 TX5n CML-I Transmitted Data Inverted	40	GND		Ground	
43 GND Ground 44 INT/RSTn Multi-Level Module Interrupt / Module Reset 2 45 VCC +3.3V Power 4 46 VCC +3.3V Power 4 47 SDA LVCMOS-I/O 2-wire Serial Interface Clock 1 48 GND Ground 4 49 TX7n CML-I Transmitted Data Inverted 50 TX7p CML-I Transmitted Data Non-Inverted 51 GND Ground 52 TX5n CML-I Transmitted Data Inverted	41	RX8p	CML-O	Receiver Data Non-Inverted	
44INT/RSTnMulti-LevelModule Interrupt / Module Reset245VCC+3.3V Power46VCC+3.3V Power47SDALVCMOS-I/O2-wire Serial Interface Clock148GNDGround49TX7nCML-ITransmitted Data Inverted50TX7pCML-ITransmitted Data Non-Inverted51GNDGround52TX5nCML-ITransmitted Data Inverted	42	RX8n	CML-O	Receiver Data Inverted	
45 VCC +3.3V Power 46 VCC +3.3V Power 47 SDA LVCMOS-I/O 2-wire Serial Interface Clock 1 48 GND Ground 49 TX7n CML-I Transmitted Data Inverted 50 TX7p CML-I Transmitted Data Non-Inverted 51 GND Ground 52 TX5n CML-I Transmitted Data Inverted	43	GND		Ground	
46 VCC +3.3V Power 47 SDA LVCMOS-I/O 2-wire Serial Interface Clock 1 48 GND Ground 1 49 TX7n CML-I Transmitted Data Inverted 50 TX7p CML-I Transmitted Data Non-Inverted 51 GND Ground 52 TX5n CML-I Transmitted Data Inverted	44	INT/RSTn	Multi-Level	Module Interrupt / Module Reset	2
47 SDA LVCMOS-I/O 2-wire Serial Interface Clock 1 48 GND Ground 49 TX7n CML-I Transmitted Data Inverted 50 TX7p CML-I Transmitted Data Non-Inverted 51 GND Ground 52 TX5n CML-I Transmitted Data Inverted	45	VCC		+3.3V Power	
48 GND Ground 49 TX7n CML-I Transmitted Data Inverted 50 TX7p CML-I Transmitted Data Non-Inverted 51 GND Ground 52 TX5n CML-I Transmitted Data Inverted	46	VCC		+3.3V Power	
49 TX7n CML-I Transmitted Data Inverted 50 TX7p CML-I Transmitted Data Non-Inverted 51 GND Ground 52 TX5n CML-I Transmitted Data Inverted	47	SDA	LVCMOS-I/O	2-wire Serial Interface Clock	1
50 TX7p CML-I Transmitted Data Non-Inverted 51 GND Ground 52 TX5n CML-I Transmitted Data Inverted	48	GND		Ground	
51 GND Ground 52 TX5n CML-I Transmitted Data Inverted	49	TX7n	CML-I	Transmitted Data Inverted	
52 TX5n CML-I Transmitted Data Inverted	50	TX7p	CML-I	Transmitted Data Non-Inverted	
	51		GND	Ground	
53 TX5p CML-I Transmitted Data Non-Inverted	52	TX5n	CML-I	Transmitted Data Inverted	
	53	TX5p	CML-I	Transmitted Data Non-Inverted	



54		GND	Ground	
55	TX3n	CML-I	Transmitted Data Inverted	
56	TX3p	CML-I	Transmitted Data Non-Inverted	
57		GND	Ground	
58	TX 1n	CML-I	Transmitted Data Inverted	
59	TX 1p	CML-I	Transmitted Data Non-Inverted	
60		GND	Ground	

Notes:

- 1. Open-Drain with pull up resistor on Host.
- 2. See pin description for required circuit.

Digital Diagnostic Specification

Parameter	Units	Min	Typical	Max	Notes
Transceiver Case Temperature	$^{\circ}\!$	-3		+3	Over operating temp
Supply voltage monitor absolute error	V	-3%		+3%	Full operating range
Channel RX power monitor absolute	dB	-3		+3	Per channel
Channel Bias current monitor	mA	- 10%		+10%	Per channel
Channel TX power monitor absolute	dB	-3		+3	Per channel



Mechanical Dimensions

